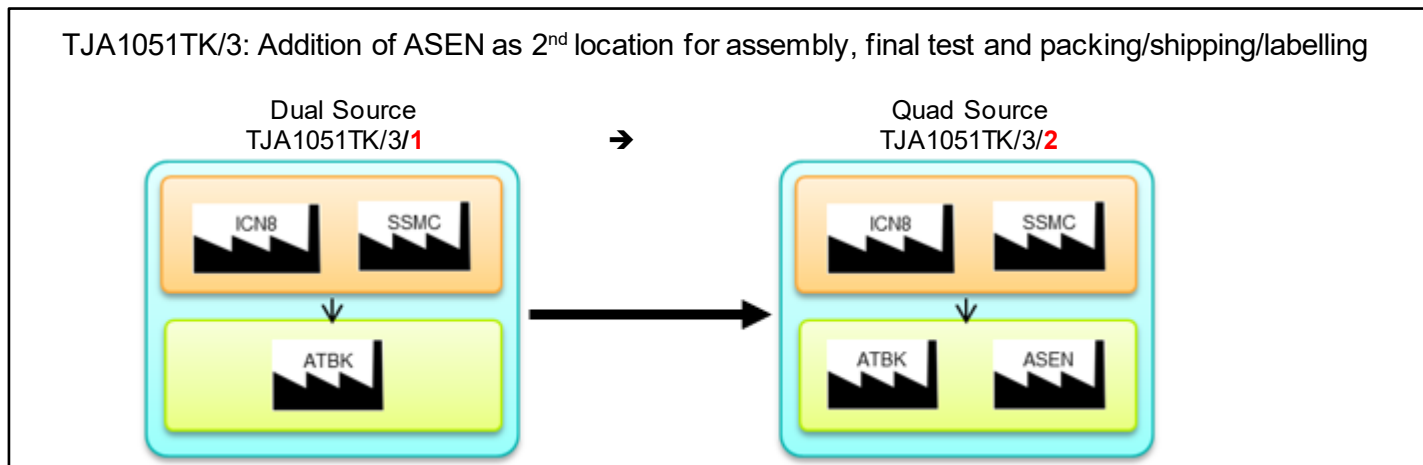


**Product Line In-Vehicle Networking (PL IVN):  
Quad Source for HVSON8 package CAN transceiver product TJA1051TK/3  
Attachment to PCN 201610016F11**



Changes for the Quad Source products with respect to the currently delivered products:

- Introduction of Dual Source Back-End (BE: assembly, Final Test (FT) and packing/shipping/labelling) in ASEN, Suzhou, China (new name ATX-SZ), next to ATBK, Bangkok, Thailand
- Industrial standardization: bondwire diameter change 20 → 18 μm
- Addition of a Shielding Bag around the reel inside the 'pizza' box

**IMPORTANT:** This document is company confidential and provided under NDA only to those direct 1<sup>st</sup> tier and distribution customers of NXP that buy or have bought one or more of the PL IVN products referred to in this document. Distribution customers are responsible for providing this document only to their 1<sup>st</sup> tier customers that buy or have bought one or more of the PL IVN products referred to in this document. NXP will not share this document with any 3<sup>rd</sup> party, and neither are 1<sup>st</sup> tier customers allowed to share this document to any 3<sup>rd</sup> party. It's the responsibility of the 1<sup>st</sup> tier customer to decide if, how, what and when they share appropriate parts of the information provided in this document to any 3<sup>rd</sup> party, e.g. their OEM customer.

Han Gerritsen  
Quality Manager PL IVN  
NXP Semiconductors

Date: May 10<sup>th</sup> 2023

Building FD3.040  
Gerstweg 2  
6534 AE Nijmegen  
The Netherlands  
E-mail: [ivn.customer.service@nxp.com](mailto:ivn.customer.service@nxp.com)

## 1. Introduction to Quad Source

As part of the NXP Business Continuity Management (BCM) program NXP's Product Line In-Vehicle Networking (PL IVN) introduces a Quad Source strategy for the leadless HVSON package CAN transceiver product TJA1051TK/3, adding Dual Source Back-End (BE) assembly, Final Test (FT) and packing/shipping/labeling in ASEN, Suzhou, China (ATX-SZ) next to ATBK, Bangkok, Thailand. This continues NXP's Global Business Continuity Management process to establish an industrial base that is agile, robust and can reliably service the long term forecasted market growth of IVN products.

Quad Source means that a product can be:

- Diffused in either waferfab ICN8, Nijmegen, the Netherlands or SSMC, Singapore
- Assembled, final tested and packed/shipped/labeled in either ATBK, Bangkok, Thailand, or ASEN, Suzhou, China

This leads to a total of four sourcing combinations. The actual sourcing is at NXP's discretion.

This change does not affect the currently released NXP PL IVN TJA1051TK/3 product versions or their 12NC ordering codes. A new 12NC ordering code will be created to make use of the Quad Source.

NXP is introducing the Quad Source option to ensure the ability to continue business operations in the event of an interruption affecting all or part(s) of the NXP organization and to establish an industrial base able to support the ever-increasing demand for PL IVN products, driven by longer term growth in the In-Vehicle Networking market. To this end, we highly recommend customers to adopt this Quad Source option.

## 2. Why do you get this change notification?

You get this change notification because you have bought or are still buying the NXP leadless HVSON8 package product TJA1051TK/3. The current NXP 12NC product ordering codes are not affected by the proposed change, the introduction of Quad Source. NXP would like to communicate in a structured way on its intended implementation of the Quad Source for the leadless HVSON8 package TJA1051TK/3 and the product qualification results for it.

## 3. Summary of the change

Product TJA1051TK/3 in the leadless HVSON8 package is released Quad Source, which implies the following changes:

- Introduction of Dual Source Back-End (BE: assembly, Final Test (FT) and packing/shipping/labelling) in ASEN, Suzhou, China, next to ATBK, Bangkok, Thailand
- Industrial standardization: bondwire diameter change 20→18 μm
- Addition of a Shielding Bag around the reel inside the 'pizza' box

For the transition Dual Source TJA1051TK/3/1 → Quad Source TJA1051TK/3/2, only a few items change:

- Single change in manufacturing site, addition of ASEN, Suzhou, China BE site next to ATBK, Bangkok, Thailand
  - In ASEN Final Test, assembly and packing/shipping/labelling will be done, like in ATBK
- No change in manufacturing flow:
  - No change in diffusion process
  - No change in assembly process
  - No change in wafer- or final test process and program
- No change in the Bill of Material (BoM), with the single exception of the bondwire diameter change 20→18 μm
- No change in packing, shipping, labeling, with the single exception of the addition of a Shielding Bag
- No change in package outline → no change in PCB footprint
- No change in leadframe → no change in solderability
- No change to the product's form, fit, function, performance, reliability and quality
- No change in the product's datasheet

On the previous two pages a high-level description of the Quad Source was given.

In the rest of this document detailed information on all aspects of the Quad Source is given in a structured and systematic way. It will answer many questions that may arise and can take away any concern over the Quad Source, which is believed to be in the interest of the customer in terms of supply chain security.

Accepting this PCN is advised to enable mid- to long-term capacity increase.

The Quad Source qualification results are described in the reliability reports that are attached to this PCN. You can obtain these reports in the same way as you obtained this document. Quad Source TJA1051TK/3/2 samples can be obtained via your NXP sales contact. Quad Source TJA1051TK/3/2 production orders can be placed, using the new NXP 12NC ordering codes described in this document.

#### **4. What information is in the rest of this document?**

Information on various aspects of the Quad Source change can be found in the following sections:

- 5. Details of the change
  - 5.1 Concept of Quad Source visualized
  - 5.2 List of TJA1051TK/3 products involved in this announcement
  - 5.3 Changes to the TJA1051TK/3 products
  - 5.4 What about wafer test?
- 6. Qualification of the change
  - 6.1 Qualification results for the assembly sourcing and bondwire diameter change
  - 6.2 Final test release in ASEN
  - 6.3 Packing/shipping/labeling in ASEN
  - 6.4 ZVEI Delta Qualification Matrices (DeQuMa)
- 7. Other topics related to the change
  - 7.1 Product Type Name and Marking
  - 7.2 Reel labeling
  - 7.3 Samples
- Appendices
  - 1. Overview of all TJA1051 product versions and previous PCNs
  - 2. Mix and match capability within Quad Source

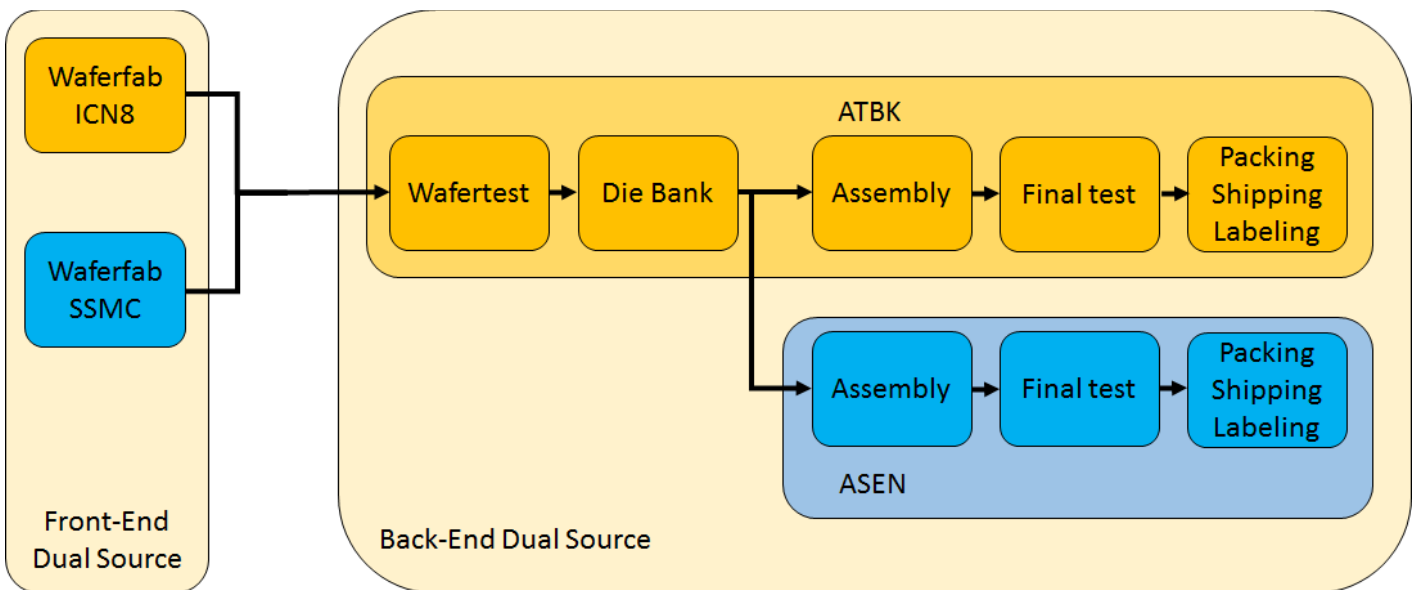
To enable better reading, here is a summary of the terms used throughout this document:

Term	Explanation
Front-End (FE) diffusion waferfab	ICN8, Nijmegen, the Netherlands or SSMC, Singapore
Back-End (BE, combination of assembly, Final Test (FT) and packing/shipping/labelling)	ATBK, Bangkok, Thailand or ASEN, Suzhou, China
Front-End Single Source (FE SS), Dual Source (FE DS)	Use of ICN8 only, use of ICN8 and/or SSMC
Back-End Single Source (BE SS), Dual Source (BE DS)	Use of ATBK only, use of ATBK and/or ASEN
Quad Source (QS)	Combination of FE DS and BE DS
Product package	The encapsulation of the product in leadless HVSON8
Product packing	The method of packing products on a reel
Bill-of-Material (BoM)	The complete set of materials and components used to make the product
Product TJA1051TK/3	Leadless HVSON package version (TK) of TJA1051. The /3 refers to the VIO version of product TJA1051, for details see the product datasheet, available from the NXP website ( <a href="http://www.nxp.com">www.nxp.com</a> ).

## 5. Details of the change

### 5.1 Concept of Quad Source visualized

In Figure 1 below the Quad Source concept is visualized. ASEN-assembled products will only be final tested and packed/shipped/labelled in ASEN, and never in ATBK. The same applies vice versa to ATBK-assembled products.



**Figure 1:** Quad Source concept, the combination of Front-End Dual Source with Back-End Dual Source.

## 5.2 List of TJA1051TK/3 products involved in this announcement

In Table 1 an overview is given of the TJA1051TK/3 products and their Quad Source versions. This PCN is about Quad Source for the leadless HVSON8 package Dual Source product TJA1051TK/3/1. The previous Single Source product TJA1051TK/3 (gray in the table) can also be transferred to Quad Source, implying acceptance of a previous PCN (see Appendix 1 on page 10).

Product	Package	Current released Product Types [1]			New Quad Source Product Type Name		
		Product Type Name	Orderable part number	Ordering code (12NC)	Product Type Name	Orderable part number	Ordering code (12NC)
TJA1051	HVSON8	TJA1051TK/3/1	TJA1051TK/3/1J	9353 035 64118	TJA1051TK/3/2	TJA1051TK/3/2Z	9353 876 43431
		TJA1051TK/3	TJA1051TK/3,118	9352 852 91118			

[1] All TJA1051TK/3 product versions mentioned in the table are released and can be ordered. This PCN is about the transition of the latest Dual Source TJA1051TK/3/1 product versions to Quad Source TJA1051TK/3/2. The previous Single Source product version TJA1051TK/3 (gray in the table) can also be transferred to Quad Source, implying acceptance of a previous PCN (see Appendix 1 on page 10).

**Table 1:** Overview of the TJA1051TK/3 product versions involved in this announcement, with explicit reference to the NXP Product Type Names, Orderable part numbers and 12NC ordering codes for the current and new Quad Source products.

## 5.3 Changes to the TJA1051TK/3/1 product

Table 2 tabulates the changes from Section 3.

Current released Product Types			Changes				
Product Type Name	Orderable part number	Ordering code (12NC)	Introduction of Dual Source BE	Introduction of Dual Source FE	bondwire diameter 20 => 18 µm	Addition of Shielding Bag	Marking format
TJA1051TK/3/1	TJA1051TK/3/1J	9353 035 64118	X	-	X	X	-
TJA1051TK/3	TJA1051TK/3,118	9352 852 91118	X	X [1]	X	X	X [1]

[1] Change previously announced, see Appendix 1 on page 10

**Table 2:** Overview of changes to products TJA1051TK/3

## 5.4 What about wafer test?

Figure 1 shows that wafer test (WT) will remain in ATBK and will not be Dual Sourced to ASEN. The reasons for this are:

- The primary reason for a multi-source strategy is to mitigate a potential supply chain risk. For WT this risk is already mitigated by having a stock-point right after WT, called a Die Bank. In this Die-Bank a stock of tested wafers is kept, awaiting call-off to assembly and final test (FT) for customer order fulfillment. This buffer Die Bank decouples the FE and BE supply chains and acts as safety stock, both of which reduce significantly any risk in the overall supply chain.
- WT equipment is rather generic, and only specific to a certain wafer diameter. The product-specific probecards can easily be interchanged among multiple WT tools. This means that WT capacity across these multiple tools is more flexible than e.g. a package-specific FT setup. This further minimizes the supply chain risk.
- The advantage of a single WT location is the single direct feedback loop to the originating waferfab on diffusion process yield (signatures). This is crucial in enabling the continuous improvement in a waferfab. The single-location buffer Die Bank after WT allows optimization of such yield feedback across various diffusion processes and products therein, while at the same time ensuring timely customer deliveries through order call-off to assembly and FT.

## 6. Qualification of the change

The change qualifications have been done according to AEC-Q100 revision G, like the original release of TJA1051TK/3 including ESD MM datasheet specification. Please download the qualification results for the diffusion sourcing change from the NXP e-PCN system you're subscribed to, on the same tab 'Files' you obtained this document from.

### 6.1 Qualification results for the assembly sourcing and bondwire diameter change

The AEC-Q100 qualification tests performed are shown in Table 3 on the next page.

Item#	Abbr.	Test	Not applicable to this change	To be considered for this change		Not applicable to TJA1051 at all	Comment
				Not applicable	Applicable		
<b>Accelerated Environment Stress Tests (AEC-Q100-REV-G)</b>							
A1	PC	Preconditioning			X		Tests are performed
A2	HAST	Highly Accelerated Stress Test			X		
A3	UHAST	Unbiased HAST	X			X	UHAST failure modes are fully covered by HAST
A4	TC	Temperature Cycling			X		Test is performed
A5	PTC	Power Temperature Cycling		X		X	For TJA1051, power <<1 Watt, DTj<400C and the device doesn't drive an inductive load. Also the wire diameter change 20=>18 mm is small
A6	HTSL	High Temperature Storage Life			X		Test is performed
<b>Accelerated Lifetime Simulation Tests (AEC-Q100-REV-G)</b>							
B1	HTOL	High Temperature Operating Life		X			No design change. All failure modes related to die-package interaction, which are relevant for an assembly site transfer, are fully covered by HAST, TC and HTSL.
B2	ELFR	Early Life Failure Rate		X			
B3	EDR	Endurance, Data Retention				X	TJA1051 doesn't contain EPROM or EEPROM
<b>Package Assembly Integrity Tests (AEC-Q100-REV-G)</b>							
C1	WBS	Wire Bond Shear			X		Tests are performed
C2	WBP	Wire Bond Pull			X		
C3	SD	Solderability			X		
C4	PD	Physical Dimensions			X		
C5	SBS	Solder Ball Shear				X	TJA1051 is an SMD device without solder balls
C6	LI	Lead Integrity				X	Only applicable for through-hole devices, TJA1051 is an SMD device
<b>Die Fabrication Reliability Tests (AEC-Q100-REV-G)</b>							
D1	EM	Electromigration	X				No change in waferfab diffusion process
D2	TDDDB	Time Dependent Dielectric Breakdown	X				
D3	HCI	Hot Carrier Injection	X				
D4	NBTI	Negative Bias Temperature Instability	X				
D5	SM	Stress Migration	X				
<b>Electrical Verification Tests (AEC-Q100-REV-G)</b>							
E1	TEST				X		Devices tested in compliance with AEC Q100-007
E2	HBM/MM	ESD Human Body Model/Machine Model	X				No design change, thus no change in any connection of the product to the outside
E3	CDM	ESD Charged Device Model			X		Test is performed
E4	LU	Latch-up	X			X	Latch-up is physically impossible in TJA1051 [1]
E5	ED	Electrical Distribution			X		Updated ED report is available
E7	CHAR	Characterization	X				Wafer- and Final Test programs, as well as test limits, remain the same
E8	GL	Gate Leakage	X				No change in waferfab diffusion process
E9	EMC	Electromagnetic Compatibility	X				No design change at all, thus also no change in the transceiver that determines the EMC response of the TJA1051 product
E10	SC	Short Circuit Characterization				X	Only applicable to smart power devices, which TJA1051 is not
E11	SER	Soft Error Rate	X			X	Only applicable to devices with >1Mbit SRAM or DRAM, which TJA1051 does not have at all
<b>Defect Screening Test (AEC-Q100-REV-G)</b>							
F1	PAT	Part Average testing			X		Sample sizes and acceptance criteria are determined in accordance with AEC-Q001 and 002
F2	SBA	Statistical Bin/Yield Analysis			X		
<b>Cavity Package Intergity Tests (AEC-Q100-REV-G)</b>							
G1 - G8			X			X	Not applicable as TJA1051 is an SMD device

**Table 3:** AEC-Q100 qualification plan for the assembly sourcing and bondwire diameter change for TJA1051TK/3.

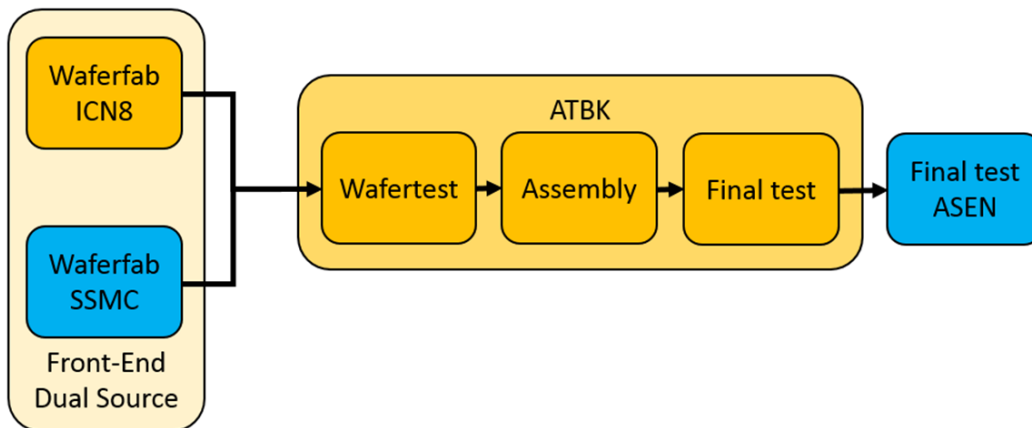
[1]: In the ABCD3 waferfab diffusion process used for TJA1051, all components are fully oxide isolated. The analog MOS transistors all have their own private back-gate contact. In the digital CMOS, the N channel transistors are fully separated from the P channel transistors. Connection to other components is through metal only. Parasitic n-p-n thyristor structures do not exist, so latch up is physically impossible.

Legend for Table 3:

- The first three columns ('Item#', 'Abbr' and 'Test') give the AEC-Q100 test number, abbreviation/acronym and description
- In the column 'Not applicable to this change', 'X' marks those tests that do not apply to this change. All the tests not marked with 'X' in this column should be considered. Of those, various tests are not required given the specific change that is being made, and others are. This is marked with 'X' in the 5<sup>th</sup> and 6<sup>th</sup> column under the heading 'To be considered for this change'.
- Various tests never apply to product TJA1051, irrespective of the change made. This is marked in the 7<sup>th</sup> column 'Not applicable to TJA1051 at all'.
- In the 'Comment' column an explanation is given where applicable
- The rows are color-coded to guide the eye:
  - Dark grey: all tests that are not applicable, either for this change or not to TJA1051 at all
  - Light grey: tests to be considered for the change, but not applicable (argument in column 'Comment')
  - White: tests performed for this change

## 6.2 Final test release in ASEN

Final test (FT) will also be Dual Sourced to ASEN, and an ASEN FT qualification report is attached to this PCN. The material flow for this ASEN FT qualification is shown in Figure 2 below.



**Figure 2:** Material flow for the ASEN FT qualification

Note that the ASEN FT qualification is completely decoupled from the ASEN assembly qualification, only material from the previously qualified ATBK assembly is used. This guarantees that ATBK and ASEN FT are equivalent, and that Quad Source products assembled and final tested in ASEN meet the same high-quality standards as those from current ATBK production.

Please download the qualification results for the ASEN Final test release from the NXP e-PCN system you're subscribed to, on the same tab 'Files' you obtained this document from.

## 6.3 Packing/shipping/labeling in ASEN

Packing/shipping/labeling will also be Dual Sourced to ASEN. Like with assembly and FT there is no cross-over of material or products from ASEN to ATBK or vice versa. Products assembled and final tested in ASEN will be packed/labeled and shipped from ASEN, and likewise for ATBK.

There are no packing, shipping or labeling differences between ASEN and ATBK, and as such the Quad Source is completely transparent to customer. A customer order on a Quad Source product can be fulfilled with any of the four possible sourcing combinations:

- ICN8/ATBK
- ICN8/ASEN
- SSMC/ATBK
- SSMC/ASEN

Within a single unit order quantity (a reel of products) there is no mixing of sources, and the reel only contains products from one of the four sourcing combinations. A single customer shipment of *multiple* unit order quantities may contain a mix of reels coming from any of the four sourcing combinations, with each reel by itself coming from a *single* sourcing combination as explained above. The actual sourcing of a reel can always be read from its label. For more information see Section 7.2.

## 6.4 ZVEI Delta Qualification Matrices (DeQuMa)

The corresponding ZVEI DeQuMa ID numbers for the changes in this PCN are:

- SEM-PA-08 for the assembly sourcing, and SEM-PA-18 for the bondwire diameter change (Section 6.1).
- SEM-TF-01 for the final test sourcing change (Section 6.2).
- Note that although there is a change in the *location* for packing/shipping/labeling, there's no change in the packing/shipping/labeling itself and therefore the associated DeQuMa ID numbers (SEM-PS) do not apply.

The ZVEI DeQuMa for the assembly, final test and bondwire diameter change for TJA1051TK/3 is attached to this PCN for reference, both in zipped excel and pdf format. It can be obtained from the NXP e-PCN system you're subscribed to, in the same way you obtained this document.

Since the original release of TJA1051 has been done with AEC-Q100 revision G, including ESD MM specification in the datasheet, the qualifications of the changes are also done according to revision G.

## 7. Other topics related to the change

### 7.1 Product Type Name and Marking

In Table 1 in Section 5.2 the Quad Source product version names are listed in the column with the heading 'New Quad Source Product Type Name'. The product name, revision number and FE/BE sourcing combination can be read from the product's top-side marking:

- 1<sup>st</sup> line : Truncated product name
- 2<sup>nd</sup> line: Diffusion and assembly batch coding for NXP traceability
- 3<sup>rd</sup> line : Coding of FE and BE site:
  - ICN8 ' → 'T'
  - SSMC → 'Z'
  - ATBK → 'n'
  - ASEN → 'X'

yww for datecode (y is last digit of year, ww is week number in that year)  
Product revision number

In Figure 3 below the change in marking is shown.

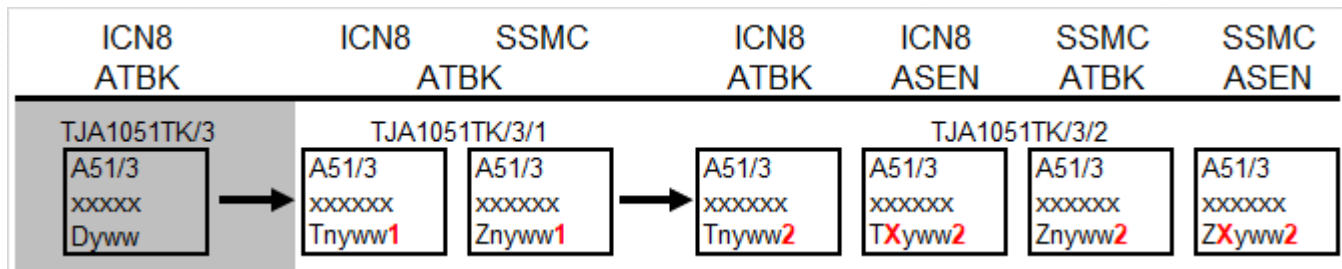


Figure 3: Change in marking for products TJA1051TK/3

For the transition Single Source TJA1051TK/3 → Dual Source TJA1051TK/3/1, which was announced to customers by NXP PCN 20131011F01 from September 2013, there was a minor change in marking format through increased numbers of characters in line B and C (line A stays the same). For the transition Dual Source TJA1051TK/3/1 → Quad Source TJA1051TK/3/2 that this PCN is about, line C marking shows the ASEN sourcing and '1' has become '2'. Within Quad Source full mix and match capability within the customer production line is guaranteed, see Appendix 2 on page 11.

### 7.2 Reel labeling

As explained in Section 7.1, the top-side marking of an individual product shows the sourcing combination in the 3<sup>rd</sup> line of marking. Each reel label shows the sourcing combination as well. In Figure 4 below example labels are shown for Quad Source product TJA1051TK/3/2. Note the sourcing combination indicated in the red boxes, with the same characters as used in the product marking (ICN8→T, SSMC→Z, ATBK→n and ASEN→X).

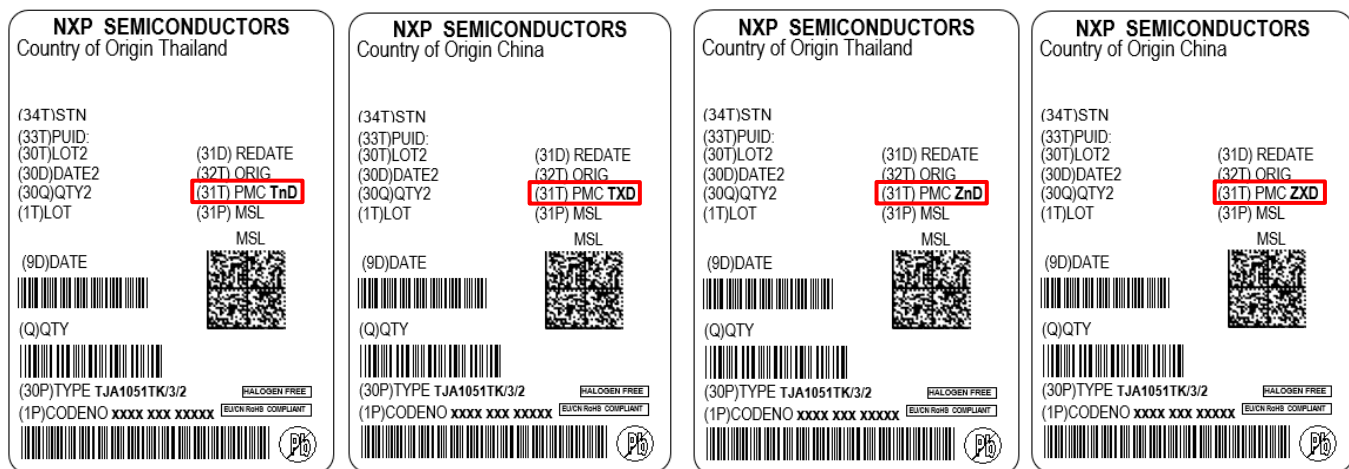


Figure 4: Example reel labels for Quad Source product version TJA1051TK/3/2

Note the Country of Origin at the top of the label, changing between Thailand (ATBK in Bangkok) and China (ASEN in Suzhou). The Country of Origin is determined by the assembly location.



## 7.3 Samples

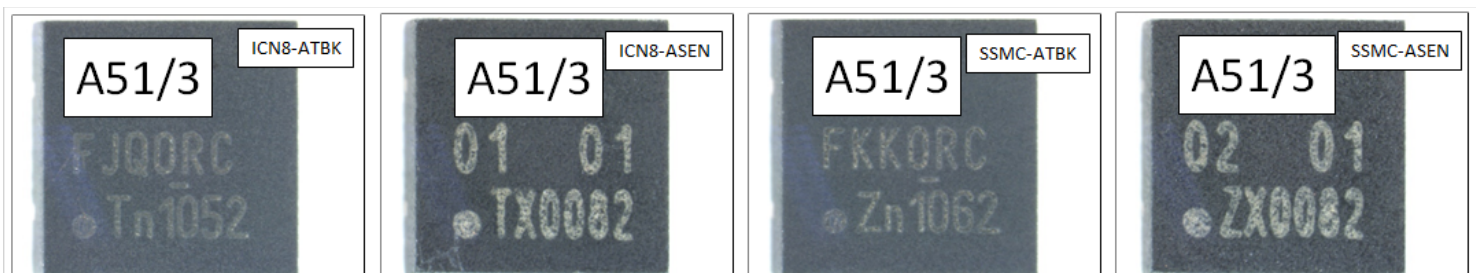
Samples for the leadless HVSON8 package TJA1051TK/3/2 Quad Source products are available. Your NXP sales contact will be able to order samples of a Quad Source product version.

In contrast to a Quad Source *production* order which can be fulfilled with a mix of sources (see Section 6.3), a Quad Source *sample* order will always be fulfilled by an equal number of samples for each of the four sourcing combinations. These four sourcing combination samples are in 4 different ESD-safe bags, each having a label that indicates its specific sourcing combination. Each Quad Source sample delivery is accompanied by a letter, explaining by reference to this label and the product's third line marking which sample is from which source combination (see Figures 5 and 6 below). This letter also refers to the NXP PCN number (201610016F11 in this case), so NXP-provided PCN documentation like this document can be easily traced back once samples are received.

The source combination of any individual sample can always be read from the 3<sup>rd</sup> line of the product marking (see Section 7.1). This enables the explicit qualification by customer of a specific sourcing combination. E.g., a customer already in production with a Front-End Dual Source product could do a delta qualification specifically on the Back-End Dual Source.



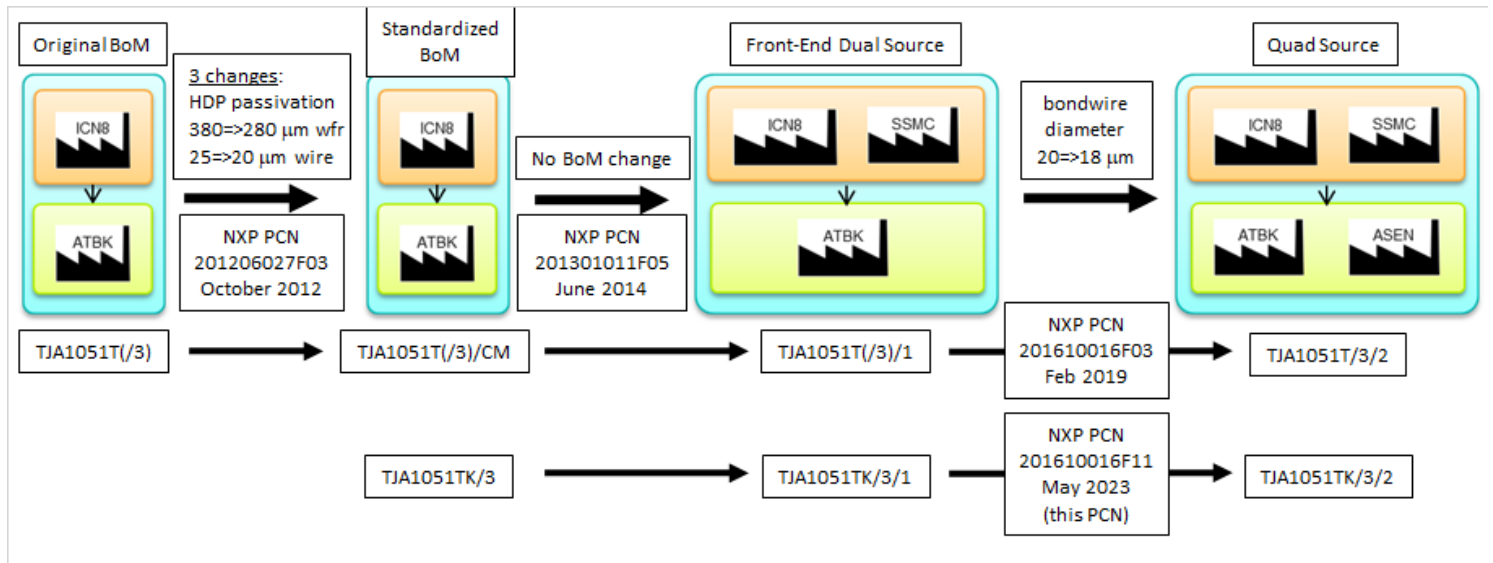
**Figure 5:** Content of any Quad Source sample shipment: four ESD-safe bags, each containing samples of one of the four sourcing combinations, and a letter explaining by reference to the sample bag labels which samples are from which source.



**Figure 6:** Products from a Quad Source sample order. The letter accompanying any Quad Source sample order (shown in Figure 5) explains the sourcing for an individual device, which can be read from the first two characters on the third line marking as explained in Section 7.1.

## Appendix 1: Overview of all TJA1051 product versions and previous PCNs

In Figure 7 below all TJA1051 product versions and the previous NXP Product Line In-Vehicle Networking (PL IVN) PCNs applicable to them are shown.



**Figure 7:** TJA1051 product versions and the previous PCNs applicable to them

There are TJA1051 product versions based on:

- SO8 package (T) or leadless HVSON package (TK)
- The /3 refers to the VIO version of product TJA1051, for details see the product datasheet, available from the NXP website ([www.nxp.com](http://www.nxp.com)).

This PCN is about the introduction of Quad Source for the leadless HVSON TJA1051TK/3 product version. Note that in 2019 already the transition to Quad Source for the SO-package TJA1051T(/3) product versions has been announced to customers by NXP 201610016F03.

## Appendix 2: Mix and match capability within Quad Source

The aim of Quad Source is to provide customers with multi-source products without hassle. It is therefore crucial that within Quad Source, products from both ATBK and ASEN can be mixed in the customer production line without any problem. Please note that:

- The Front-End Diffusion Dual Source, implied in Quad Source, obviously has no impact on the product appearance
- An ATBK-ASEN change-over, or vice versa, only appears per reel unit (Section 6.3)

This mix and match capability within Quad Source in the customer production line is determined by product packing, marking format and appearance, package and lead outline and dimensions, solderability and traceability.

### Product packing

Product packing contains cavity and cover tape the reel, the reel box and labeling and the shipment outer box.

There are no differences, except for:

- The label content mentioned in Section 7.2, between ATBK and ASEN Quad Source products, enabling mixing in the customer production line.
- The additional Shielding Bag around the reel in the 'pizza' box is put in to be more robust against poor customer storage conditions, which in specific cases we have become aware of.

### Marking format and appearance

Within the Quad Source products, the marking format and appearance is exactly the same for all four sourcing combinations including the added ASEN BE source (see Figure 3 in Section 7.1). This enables full mix and match use of all four sourcing combinations in the customer production line without any impact on potentially customer-performed Automatic Optical Inspection (AOI).

For the transition Dual Source TJA1051TK/3/1 → Quad Source TJA1051TK/3/2 the marking format and appearance doesn't change for the added ASEN BE source (see Figure 3 in Section 7.1). The transition can be made without any impact on potentially customer-performed AOI.

For the transition Single Source TJA1051TK/3 → Quad Source TJA1051TK/3/1 the marking appearance doesn't change, but the format slightly changes through the additional characters in line B and C (see Figure 3 in Section 7.1). NXP can not judge whether there is any impact for the customer when transferring from current (ATBK only) products to the Quad Source (ATBK and ASEN) products. This obviously depends on whether or not customer actually performs PCB AOI, and if so what settings or boundary conditions are used.

### Package and lead outline and dimensions

The package and lead outline and dimensions of both ATBK and ASEN Quad Source products comply with the same product outline/dimension specification, as given in the product's datasheet. See Figure 8 on the next page for leadless HVSON8.

This means that both ATBK and ASEN products can be handled by the same pick-and-place machine, use the same footprint, and can therefore be mixed in the customer production line.

### Solderability

As the lead outline, dimensions and material are the same between ATBK and ASEN, there is no impact to solderability and both products can be mixed in the customer production line without impact.

### Traceability

Product top-side marking (Section 7.1) and reel labeling (Section 7.2) of Quad Source products enables the same traceability in the customer production line as for any of the currently delivered Single Source or Dual Source products. At NXP side this holds equally, the traceability for Quad Source products within either Front-End diffusion or Back-End assembly site is equivalent to that of current Single Source or Dual Source products.

Taking all previous information into account, Quad Source products are completely transparent to customers.

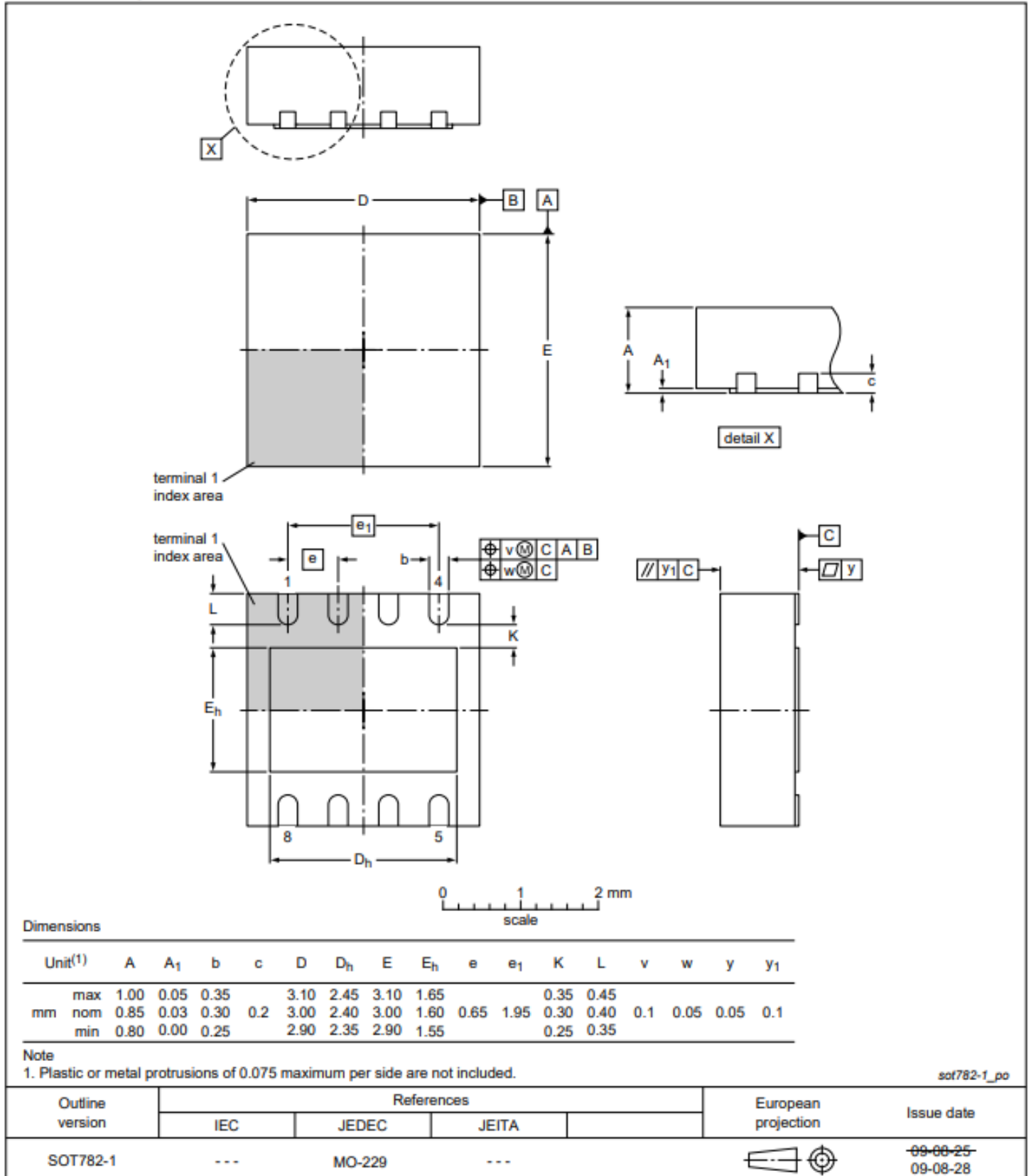


Figure 8: Leadless HVSON8 physical outline/dimension specification, as shown in the TJA1051 datasheet